

# Ultralow Resistance Ohmic Contacts for p-Channel InGaSb Field-Effect Transistors

Luke W. Guo, Wenjie Lu, Brian R. Bennett, John Brad Boos, and Jesús A. del Alamo, *Fellow, IEEE*

**Abstract**—We demonstrate ultralow ohmic contact resistance to antimonide-based, p-channel quantum-well field-effect transistor (QW-FET) structures using a new p<sup>+</sup>-InAs/InAsSb cap structure. The incorporation of a p<sup>+</sup>-InAsSb layer enables the use of a thicker cap with lower sheet resistance, resulting in an improved contact resistivity. Using a Pd-based ohmic scheme, the composite cap structure resulted in a 4× reduction in contact resistance compared with a standard p<sup>+</sup>-InAs cap. This translates into nearly 3× improvement in the  $g_m$  of fabricated InGaSb p-channel QW-FETs. Furthermore, Ni contacts on the composite cap were fabricated and a contact resistance of 45  $\Omega \cdot \mu\text{m}$  was obtained. An accurate contact resistivity extraction in this very low range is possible through nanotransmission line models with sub-100 nm contacts. In devices of this kind with Ni-based contacts, we derive an ultralow contact resistivity of  $5.2 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ .

**Index Terms**—Antimonide, nano contacts, TLM, contact resistivity, quantum-well FET, nano-TLM.

## I. INTRODUCTION

III-V MATERIALS have attracted considerable interest for integration into future complementary metal-oxide-semiconductor (CMOS) technology due to their outstanding electron transport properties [1]. Recently demonstrated III-V n-channel MOSFETs have shown great promise towards the development of high-performance devices with small footprint, excellent electrostatic integrity, and low parasitic resistance [2]. However, less progress has been made in developing p-channel transistors due to lower hole mobility of most III-V compound semiconductors.

A notable exception is the antimonide material system, which has recently attracted considerable attention. Significant progress has been made towards antimonide-based p-channel MOSFETs [3]–[5], including the demonstration of high-k dielectrics [6] as well as the incorporation of biaxial [7]–[9] and uniaxial strain [10], which has been shown to greatly enhance transport characteristics [11]. However, one of the challenges hampering the development of high-performance III-V p-channel MOSFETs is the lack of

a low-resistance ohmic contact technology. In this regard, InAs is a common cap material for antimonide FETs due to the high etching selectivity that it presents with respect to other antimonide compounds. To our knowledge, the best reported contact resistivity on p<sup>+</sup>-InAs is  $1.6 \cdot 10^{-6} \Omega \cdot \text{cm}^2$  using Pd contacts [12]. While there are low-resistance contacts for n-type FETs with n<sup>+</sup>-InAs caps [13], the contact resistance on p<sup>+</sup>-InAs is inadequate to meet the needs of a future nanoscale CMOS technology.

In this work, ohmic contacts for InGaSb FETs using a novel p<sup>+</sup>-InAs/InAsSb composite cap are fabricated and characterized. The motivation for this new cap structure stems from the lattice mismatch that typically exists between the InAs cap and the InGaSb channel, which has an InSb composition that ranges from 20% to 40%. The resulting 1.2% to 3.2% lattice mismatch limits the InAs cap thickness. Thicker caps develop a large density of defects that yield a poor contact resistance. To address this problem, we introduce a thick p<sup>+</sup>-InAsSb subcap that is lattice-matched to the channel under a thin p<sup>+</sup>-InAs surface layer. This maintains a high crystallographic quality through the entire cap, resulting in better electrical characteristics.

In this letter, we show that the new cap design results in very large improvements in the contact resistance of Pd-based ohmic contacts to FET-type structures. This improved contact resistance translates into InGaSb QW-FETs with greatly enhanced electrical characteristics. In addition, an ultralow contact resistivity of  $5.2 \cdot 10^{-8} \Omega \cdot \text{cm}^2$  using a Ni/Pt/Au ohmic metal scheme is demonstrated.

## II. Pd OHMIC CONTACTS AND TRANSISTOR CHARACTERIZATION

Two InGaSb QW-FET heterostructures were grown by molecular beam epitaxy on GaAs substrates [7]. Fig. 1(a) shows a cross-section of one of them which features a highly-doped p-type InAs/InAs<sub>0.85</sub>Sb<sub>0.15</sub> 5/30 nm bilayer cap ( $N_A = 1 \times 10^{19} \text{ cm}^{-3}$  for both layers). The second heterostructure is identical, except for the cap, which is comprised of a 20 nm InAs single-layer with the same doping.

Conventional and circular transmission line model (TLM and CTLM, respectively) test structures were fabricated to characterize various ohmic contact schemes. The samples are first cleaned with organic solvents and patterned with photoresist. They are then ashed for 5 minutes in oxygen plasma to remove residual resist and dipped in 10% HCl to remove the native oxide. The samples are immediately transferred to an electron-beam deposition system and

Manuscript received March 11, 2015; revised April 1, 2015; accepted April 6, 2015. Date of publication April 9, 2015; date of current version May 20, 2015. This work was supported by Samsung and Intel Corporation. The review of this letter was arranged by Editor R. Quay.

L. W. Guo, W. Lu, and J. A. del Alamo are with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: wenjie@mit.edu).

B. R. Bennett and J. B. Boos are with the Electronics Science and Technology Division, U.S. Naval Research Laboratory, Washington, DC 20375 USA.

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2015.2421337

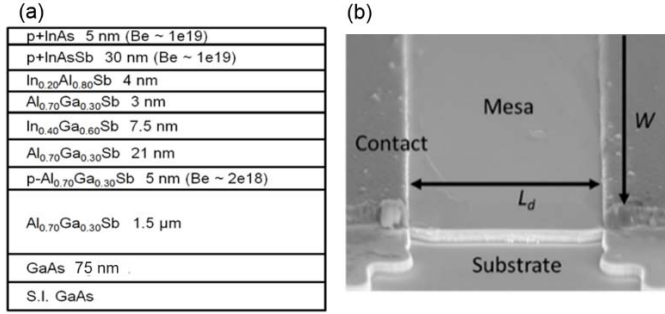


Fig. 1. (a) Schematic of heterostructure with p<sup>+</sup>-InAs/In<sub>0.85</sub>As<sub>0.15</sub>Sb composite cap layer. (b) SEM picture of a fabricated TLM structure with Ni/Pt/Au (15/10/100 nm) contacts that are 6 μm apart.

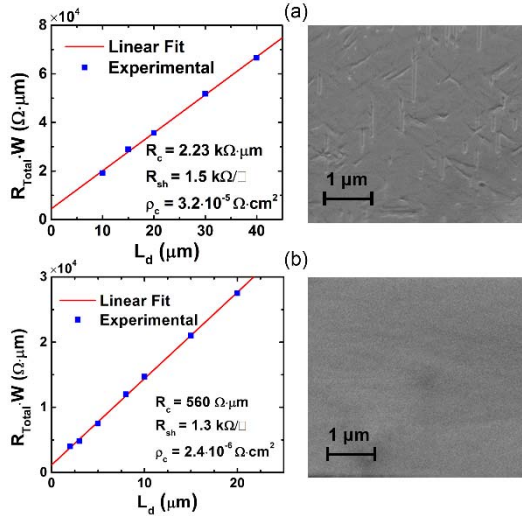


Fig. 2. Electrical measurements (left) and SEM pictures of virgin semiconductor surface (right) on Pd/Pt/Au TLMs on: (a) p<sup>+</sup>-InAs cap structure, and (b) p<sup>+</sup>-InAs/InAsSb cap structure.

brought to vacuum. Metal contacts are subsequently deposited and lifted-off. Mesa isolation is then performed by means of BCl<sub>3</sub> plasma etching. Finally, sequential annealing at increasing temperature is carried out on each sample in N<sub>2</sub> in 3 min steps. Samples are placed upside down on a GaAs proximity cap to prevent surface decomposition [14].

In addition to these TLM structures, nano-TLMs were also fabricated for accurate extraction of low contact resistivities [15]. Nano-scale Ni contacts are lifted-off using PMMA as electron-beam resist. Figs. 1(b) and 4(c) show examples of finished TLM and nano-TLM test structures. Test structure characterization is performed using four-point probe measurements. Results obtained from TLMs and CTLMs were found to be consistent. All sample dimensions were measured by SEM to ensure accuracy in extracting low values of  $R_c$ .

Fig. 2 shows TLM data for Pd/Pt/Au (10/10/150 nm) contacts on both heterostructures, annealed at 200°C. The sample with the InAs single-layer cap exhibits  $R_c$  of 2.23 kΩ · μm and  $R_{sh}$  of 1.56 kΩ/□, while the InAs/InAsSb bilayer yields  $R_c$  of 560 Ω · μm and  $R_{sh}$  of 1.32 kΩ/□, representing a 4X improvement in the contact resistance. 200 °C was selected as optimum annealing temperature based on the literature [16] and our own sequential annealing experiments (Fig. 4(b)).

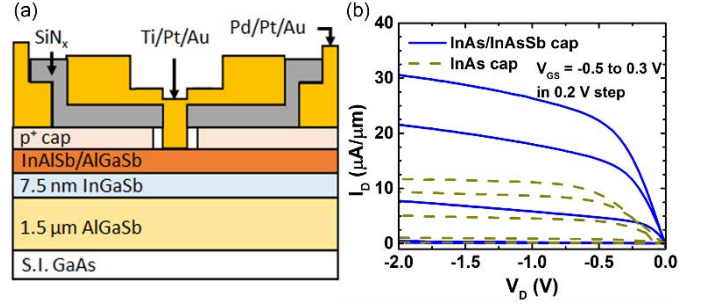


Fig. 3. (a) Schematic cross-section of InGaSb p-channel QW-FETs fabricated in this work. Device heterostructure is the same as in Fig. 1(a). (b) Output characteristics of  $L_g = 0.5$  μm InGaSb QW-FETs with both cap designs.  $V_{GS}$  is swept from -0.5 V to 0.3 V, in -0.2 V steps.

The improvement in the contact resistance in the composite cap is likely due to its better crystallographic quality. SEM examination of the sample with the pure InAs cap reveals a surface with line defects, as shown in Fig. 2(a), presumably due to excessive tensile stress in the InAs layer. Use of a lattice-matched InAsSb sub-cap mitigates the stress and results in a smooth surface (Fig. 2b). To verify that the observed defects in the InAs cap sample were limited to the cap, the InAs layer was removed in a 3:1 citric acid/H<sub>2</sub>O<sub>2</sub> solution, with the 4 nm InAlSb layer serving as an etch stop. The exposed surface underneath was smooth and free of the line defects.

To confirm the device worthiness of the new cap design, InGaSb p-channel QW-FETs with  $L_g = 0.5$  μm using both cap structures were fabricated. Fig. 3(a) shows a cross-section of the finished device. After standard cleaning, Pd/Pt/Au contacts are deposited lifted-off and annealed at 200°C as in the TLM process. Then, 50 nm of SiN<sub>x</sub> is deposited via PECVD. The 0.5 μm gate opening is defined by electron-beam lithography and the dielectric is patterned by SF<sub>6</sub>/O<sub>2</sub> plasma etching. The cap is recessed in 3:1 citric acid/H<sub>2</sub>O<sub>2</sub> solution. The Ti/Pt/Au metal gate is patterned and deposited by electron-beam evaporation and lifted-off. Finally, mesa etch is done using lactic acid/H<sub>2</sub>O<sub>2</sub> wet etch.

Fig. 3(b) shows the output characteristics of a finished InGaSb QW-FET. The device with the composite cap exhibits a drain current that is more than double that of the device with the InAs-only cap. Both devices have ungated region of 2 μm on both sides of the channel. The InAs cap sample has  $R_{on}$  of 34.4 kΩ · μm and a peak  $g_m$  of 26 mS/mm (at  $V_D = -2$  V). By contrast, the bilayer cap sample has  $R_{on}$  of 12.8 kΩ · μm and peak  $g_m$  of 72 mS/mm (at  $V_D = -2$  V). These results demonstrate that the greatly improved contact resistance obtained in the new cap structure does translate into major enhancements in device electrical characteristics.

### III. Ni OHMIC CONTACTS AND NANO-TLM CHARACTERIZATION

It has recently been shown that Ni alloyed contacts are promising candidates for FETs using both n<sup>+</sup>-InAs [17] and p<sup>+</sup>-GaSb [18] cap structures. This motivates us to explore Ni/Pt/Au (15/10/100 nm) contacts on the new

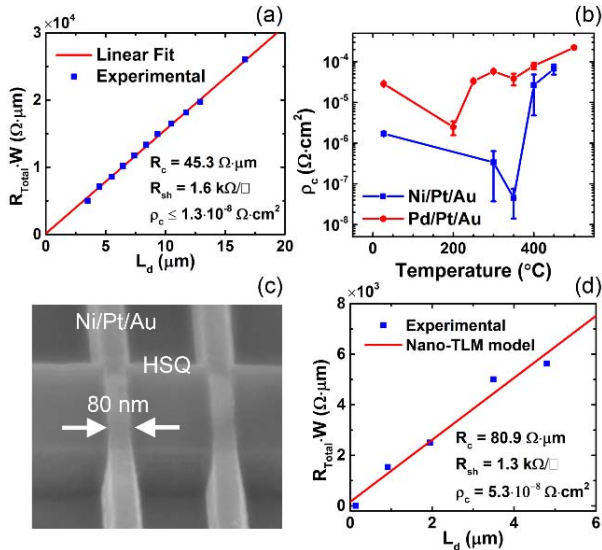


Fig. 4. (a) Electrical measurements on a CTLM with Ni/Pt/Au contacts on the  $p^+$ -InAs/InAsSb cap structure after 3 min 350 °C annealing. (b) Evolution of contact resistivity of Pd/Pt/Au and Ni/Pt/Au contacts in a sequential annealing (3 min) experiment. (c) SEM image of a Ni/Pt/Au nano-TLM test structure, with 80 nm contact length, 130 nm contact spacing, and 1  $\mu\text{m}$  width. (d) Electrical measurements in nano-TLMs with nano-contacts with average  $L_c$  of 100 nm.

InAs/InAsSb cap structure. Fig. 4(b) shows CTLM resistance measurements and the extracted value of  $\rho_c$  in sequential annealing experiments. At 350 °C, as shown in Fig. 4(a), we obtained the lowest contact resistance of  $45.3 \Omega \cdot \mu\text{m}$ . This corresponds to  $\rho_c = 1.3 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ . Above 350 °C, the metal starts to delaminate and the contact resistance increases rapidly. Similar contact resistance degradation at around this temperature has also been observed in the Ni-InGaAs contact system [19], [20]. In 6 sets of test structures consisting of a total of 72 CTLMs, the average  $\rho_c$  obtained after 350 °C anneal is  $4.5 \cdot 10^{-8} \Omega \cdot \text{cm}^2$  with a standard deviation of  $3.1 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ . The average  $R_c$  is  $70 \Omega \cdot \mu\text{m}$ .

To confirm these results, we also fabricated nano-TLMs with contacts as small as  $L_c = 80 \text{ nm}$  and contact separation down to  $L_d = 130 \text{ nm}$ . Fig. 4(d) shows measurements of nano-TLMs with nano-contacts of average measured  $L_c$  of 100 nm. Because  $R_{||}$  and  $R_{\times}$  differ by less than 1%, only data for  $R_{||}$  are shown. From them, we can extract an average  $R_c$  of  $82.7 \Omega \cdot \mu\text{m}$  (for  $L_c > L_T$ ) and an average  $\rho_c$  of  $5.2 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ , with standard deviations of  $10 \Omega \cdot \mu\text{m}$  and  $2.4 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ , respectively. This, to the author's knowledge, is the lowest reported contact resistivity to p-type InAs.

The work of Oxland *et al.* indicates that under similar conditions to ours, Ni on InAs forms a shallow reaction region of 7 nm depth [17]. This suggests that the top InAs layer in our cap structure is mostly consumed in the reaction and that a direct contact exists between the reacted region and the underlying InAsSb layer. This might be the key behind these excellent results.

#### IV. CONCLUSIONS

Ohmic contacts for p-type antimonide-based devices have been studied using a new InAs/InAsSb bilayer cap structure.

We demonstrate a significant enhancement of contact resistance and on-resistance in Pd ohmic contacts and InGaSb QW-FETs. Furthermore, an ultralow contact resistivity of  $5.2 \cdot 10^{-8} \Omega \cdot \text{cm}^2$  was obtained with Ni alloyed contacts. Our results suggest that the use of self-aligned Ni-based contacts coupled with the new cap structure should enable a new class of antimonide-based p-type FETs with outstanding performance.

#### REFERENCES

- [1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011.
- [2] J. Lin *et al.*, "A new self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process," in *Proc. IEEE IEDM*, Dec. 2013, pp. 16.2.1–16.2.4.
- [3] M. Barth *et al.*, "Compressively strained InSb MOSFETs with high hole mobility for p-channel application," in *Proc. 71st Annu. DRC*, Jun. 2013, pp. 21–22.
- [4] M. Xu, R. Wang, and P. D. Ye, "GaSb inversion-mode PMOSFETs with atomic-layer-deposited  $\text{Al}_2\text{O}_3$  as gate dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 883–885, Jul. 2011.
- [5] A. Nainani *et al.*, "Development of high- $k$  dielectric for antimonides and a sub 350 °C III-V pMOSFET outperforming germanium," in *Proc. IEEE IEDM*, Dec. 2010, pp. 6.4.1–6.4.4.
- [6] A. Nainani *et al.*, "Optimization of the  $\text{Al}_2\text{O}_3/\text{GaSb}$  interface and a high-mobility GaSb pMOSFET," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3407–3415, Oct. 2011.
- [7] B. R. Bennett *et al.*, "Mobility enhancement in strained p-InGaSb quantum wells," *Appl. Phys. Lett.*, vol. 91, no. 4, p. 042104, Jul. 2007.
- [8] J. B. Boos *et al.*, "High mobility p-channel HFETs using strained Sb-based materials," *Electron. Lett.*, vol. 43, no. 15, pp. 834–835, Jul. 2007.
- [9] M. Radosavljevic *et al.*, "High-performance 40 nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power ( $V_{CC} = 0.5 \text{ V}$ ) logic applications," in *Proc. IEEE IEDM*, Dec. 2008, pp. 1–4.
- [10] L. W. Guo *et al.*, "Enhancing p-channel InGaSb QW-FETs via process-induced compressive uniaxial strain," *IEEE Electron Device Lett.*, vol. 35, no. 11, pp. 1088–1090, Nov. 2014.
- [11] L. Xia *et al.*, "Hole mobility enhancement in  $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$  quantum-well field-effect transistors," *Appl. Phys. Lett.*, vol. 98, no. 5, p. 053505, Jan. 2011.
- [12] E. M. Lysczek, J. A. Robinson, and S. E. Mohney, "Ohmic contacts to p-type InAs," *Mater. Sci. Eng., B*, vol. 134, no. 1, pp. 44–48, Sep. 2006.
- [13] R. Dormaier *et al.*, "Thermal stability of Pd/Pt/Au ohmic contacts to InAlSb/InAs heterostructures for high electron mobility transistors," *J. Appl. Phys.*, vol. 105, no. 4, pp. 044505-1–044505-8, Feb. 2009.
- [14] J. A. del Alamo and T. Mizutani, "Rapid thermal annealing of InP using GaAs and InP proximity caps," *J. Appl. Phys.*, vol. 62, no. 8, pp. 3456–3458, Oct. 1987.
- [15] W. Lu *et al.*, "A test structure to characterize nano-scale ohmic contacts in III-V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 178–180, Feb. 2014.
- [16] J. B. Boos *et al.*, "Ohmic contacts in AlSb/InAs high electron mobility transistors for low-voltage operation," *J. Vac. Sci. Technol. B*, vol. 17, no. 3, pp. 1022–1027, May 1999.
- [17] R. Oxland *et al.*, "An ultralow-resistance ultrashallow metallic source/drain contact scheme for III-V NMOS," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 501–503, Apr. 2012.
- [18] Z. Yuan *et al.*, "Antimonide-based heterostructure p-channel MOSFETs with Ni-alloy source/drain," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1367–1369, Nov. 2013.
- [19] L. A. Walsh *et al.*, "Ni-(In,Ga)As alloy formation investigated by hard-X-ray photoelectron spectroscopy and X-ray absorption spectroscopy," *Phys. Rev. Appl.*, vol. 2, no. 6, p. 064010, Dec. 2014.
- [20] L. Czornomaz *et al.*, "CMOS compatible self-aligned S/D regions for implant-free InGaAs MOSFETs," *Solid-State Electron.*, vol. 74, pp. 71–76, Aug. 2012.